# A Study on Noise Reduction in CMOS Image Sensors using High-Gain Front-end Readout Circuits

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Abstract of Doctoral Thesis

Title of Thesis: A Study on Noise Reduction in CMOS Image Sensors using High-Gain Front-end Readout Circuits

Abstract:

Recent advances in CMOS image sensor technology such as the use of pinned photodiodes have indicated the possibility of realizing high-sensitivity CMOS image sensors. Amplification of the read signal by a high-gain front-end readout circuit at each column is another technology that enhances the sensitivity of CMOS image sensors. The insertion of high-gain column readout circuits directly reduces read noise attributable to the output buffer amplifier at the final stage, as well as quantization noise from the analog/digital (A/D) converter. In addition to these effects, the high-gain column readout circuits may also reduce the temporal noise due to in-pixel source followers. The temporal noises of the in-pixel source followers are categorized into thermal, 1/f and random telegraph signal (RTS) noises. There have been several researches treating thermal and 1/f noise reduction techniques using high-gain readout circuits of CMOS image sensors. However, the reduction of the RTS noise using high-gain column readout circuits is not well investigated and the reduction of the RTS noise is still a big issue for the development of high-sensitivity CMOS image sensors for low light level applications. Efficient implementation techniques of the high-gain column readout circuits if an A/D converter is co-integrated at the column are not well discussed so far.

In this thesis, noise reduction in CMOS image sensors using high-gain front-end readout circuits have been studied and proposed. The study focuses
on

(1) efficient implementation of high-gain column amplifiers co-integrated with column A/D converters,
(2) histogram-based RTS-noise reduction techniques and
(3) amplifier-selection pixels and correlated multiple sampling techniques.

A column parallel analog-to-digital converter (ADC) with an embedded programmable gain amplifier (PGA) for high-speed low-noise wide dynamic range CMOS image sensors is proposed in this thesis. It uses a modified cyclic ADC circuit topology where a set of capacitors are controlled to obtain an optimum gain for noise suppression. Results from this technique show the effectiveness of the embedded PGA for reduction of ADC non-linearity and random noise. Low random noise can be obtained by increasing the gain. The gain accuracy obtained for all PGA gain configuration are less than 0.5%. It shows that the noise level at lower gain effectively decreases as gain increases.

Histogram-based RTS noise suppression and averaging (HRS) is used in column parallel signal processing technique to reduce RTS noise of in-pixel source follower. In this method, a histogram with multiple samples of signal and reset voltage used to estimate the amplitude of the RTS noise. With the median of the histogram and the estimated amplitude, the RTS noise components are removed and the average is calculated with the histogram. This effectively reduces thermal noise. Results show for a sampling number equal to 128, input-referred noise is reduced to 48µV for slow relaxation RTS noise waveform.

A noise reduction technique with selectable dual source followers has also been studied. Each pixel has two selectable transistors where the lower-noise transistor is chosen for reading signal. A prototype with 65x290 pixels for demonstrating the effectiveness of this technique has been implemented. The measured result of in-chip processing shows that the mean noise amplitude using the amplifier-selection technique at the cumulative probability of 6x10⁻⁵ is reduced to 9.6e- from 17.2e- which is the noise level using one of the amplifiers without selection.